MULTIMEDIA UNIVERSITY

STUDENT ID NO

MULTIMEDIA UNIVERSITY

FINAL EXAMINATION

TRIMESTER 2, 2022/2023

EEN1036 - DIGITAL LOGIC DESIGN

(TE/RE)

10 JULY 2023
9.00 a.m - 11.00 a.m.
(2 Hours)

INSTRUCTION TO STUDENT

1. This question paper consists of 5 pages (including the cover page) with 4 questions.

2. Attempt **ALL** questions. All questions carry equal marks and the distribution of the marks for each question is given.

3. Please write all your answers in the Answer Booklet provided.

QUESTION 1

(a) Convert the following number from the given base to the other bases listed in Table Q1 (correct to 3 decimal places). Show your workings.

Table Q1

Decimal	Binary	Octal	Hexadecimal
?	?	?	A6B8.F

[6 marks]

(b) Subtract 252_{10} from 138_{10} in 2's complement system by using 8 bits (including the sign bit) for each number. Verify your results by decimal arithmetic.

[4 marks]

(c) Convert 65_{10} and 58_{10} to Binary Coded Decimal (BCD) numbers and add these numbers using BCD addition. Verify your results by decimal arithmetic.

[3 marks]

(d) Your lecturer keeps her final exam scripts in her office. She would like you to design an alarm system for her office for security reasons. The office has a window and door that are equipped with sensors that produce a HIGH on input A and B respectively. When the alarm system is turned on with a key, a siren should sound when at least the window or the door is open.

i. Construct a truth table for the alarm system.

[4 marks]

ii. Write out the standard sum-of-products (SOP) expression for the alarm system.

[2 marks]

iii. Simply the Boolean expression in (ii) using Boolean algebra.

[2 marks]

iv. Simply the Boolean expression in (ii) using a Karnaugh map (K-map).

[4 marks]

Continued...

QUESTION 2

(a) Given a logic circuit as shown in Figure Q2(a),

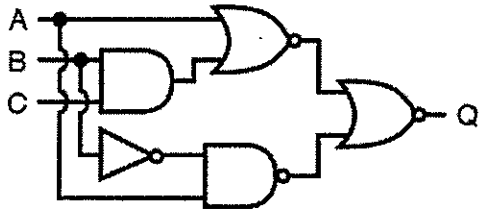

Figure Q2(a)

i. Determine the Boolean expression for the circuit.

ii. Using DeMorgan's Theorem, prove that the simplified Boolean expression is $Q = A\overline{B}$

iii. Using the simplified Boolean expression, implement the logic network by using only NOR gates.

iv. Demonstrate how a K-map can be used to obtain the simplified expression in (ii). Show your workings.

[3 + 4 + 6 + 4 marks]

(b) From the truth table in Figure Q2(b) below, derive the simplified product-of-sum (POS) expression using a K-map.

Input				Output
A	**B**	**C**	**D**	**Y**
0	0	0	0	0
0	0	0	1	1
0	0	1	0	0
0	0	1	1	1
0	1	0	0	X
0	1	0	1	0
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	X
1	0	1	0	0
1	0	1	1	X
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

Figure Q2(b)

[8 marks]

Continued...

QUESTION 3

(a) Implement a synchronous modulo-6 down counter using the positive edge-triggered JK flip-flops.

i. Draw the state transition diagram of the synchronous down counter above.

ii. List the J-K Flip Flop transition table.

iii. Construct the state table based on (i).

iv. Draw the Karnaugh map and simplify the logical expression of each J and K of each flip flop.

v. Draw the logic circuit of the asynchronous modulo-6 up counter accordingly.

[2 + 1 + 3 + 6 + 3 marks]

(b) Name two types of random-access memory and their corresponding storage elements.

[4 marks]

(c) Determine the output states for this D flip-flop, given the pulse inputs as shown in Figure Q3 below.

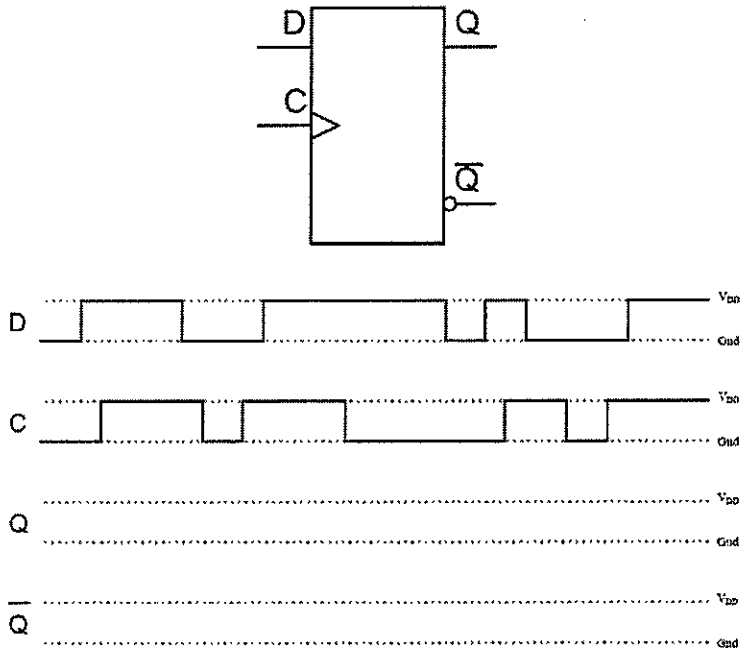

Figure Q3

[6 marks]

Continued...

QUESTION 4

(a) List two types of IC technologies that are most widely used. [2 marks]

(b) Which IC technology generally has the lowest power dissipation and why? [3 marks]

(c) Define an Arithmetic Logic Unit. [2 marks]

(d) The truth table of Decimal to BCD encoder is given in Figure Q4(d) below:

	BCD Code			
Decimal	**A3**	**A2**	**A1**	**A0**
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

Figure Q4 (d)

i. Write the logic equation of A3, A2, A1 and A0 using sum of minterms. [8 marks]
ii. Implement the Decimal to BCD encoder using the OR gate. [4 marks]

(e) Provide the definitions for "multiplexer" and "demultiplexer". [4 marks]

(f) For Figure Q4(f) below, identify if the schematic refers to "multiplexer" or "demultiplexer".

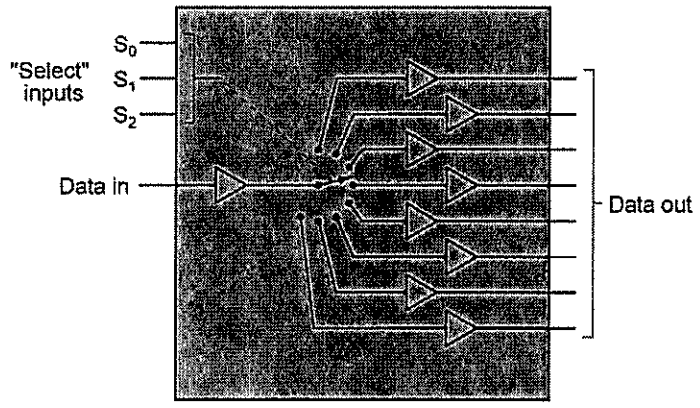

Figure Q4(f)

[2 marks]

End of Paper